REMARKS

In the Office Action, claims 41-45, 47-54 and 56-57 are rejected under 35 U.S.C. §103(a) as being unpatentable over Venkateshwaran et al. in view of Akram et al., claims 46 and 55 are rejected under 35 U.S.C. §103(a) as being unpatentable over Venkateshwaran et al. in view of Akram et al. and further in view of Chiang et al.

Claims 46 and 55 are cancelled. The two base claims 41 and 49 are amended to further clearly define the invention in a patentable way to overcome the rejections under 35 U.S.C. §103(a). Specifically, the amended independent claim 41 now includes the limitation that the multi-chip package structure comprises **at least two chip packages, each of said chip packages being a packaged chip module having a bare chip packaged and embedded therein, burn-in tested and function tested**. Similarly, the amended independent claim 49 includes the limitation that the multi-chip package structure comprises **at least a bare chip and at least one chip package, said chip package being a packaged chip module having a bare chip packaged and embedded therein, burn-in tested and function tested**.

Applicants like to point out that **a bare chip is a semiconductor die cut from a wafer. A bare chip or a semiconductor die is different from a packaged chip module** of this invention in that a packaged chip module is a finished chip package that comprises a bare die embedded within, burn-in tested and function tested. **In other words, a packaged chip module is a protected module which has a good die embedded therein**

and guaranteed to be functional but a bare chip is not protected and may be already defective.

There are several advantages in using a packaged chip module rather than a bare chip in packaging a multi-chip module. One is that it avoids the possibility of packaging a bare chip that may not be functional at all in the first place. The other is that the packaged chip module is much better protected than a bare chip from being damaged during the multi-chip packaging process. Because a multi-chip module comprises multiple chips and is usually a high cost product, having high yield is very important in manufacturing. **None of the prior arts including those cited by the Examiner has ever taught, suggested or anticipated the use of a packaged chip module in packaging a multi-chip module.**

As pointed out in the specification and the remarks in the response to a previous office action, the gist of this invention is to provide a multi-chip package structure that integrates at least an **already packaged and tested chip module onto the substrate of the multi-chip package structure**. By integrating a packaged chip module, the yield of the multi-chip package is greatly increased because the **packaged chip module has passed both burned-in and function test**. The unique technique of the instant invention has not been known and practiced in the industry and has provided significant improvement in high yield and benefit for manufacturing a multi-chip module.

Venkateshwaran et al. teach a stacked multi-chip assembly including a plurality of **integrated circuit die** directly attached to a substrate having pads corresponding to terminals on the die, and interconnections between the die, and also to external contacts.

Throughout the disclosure of Venkateshwaran et al., it is clearly indicated that **a die** 201 (col. 1, line 58) or **integrated dices** (col. 3, lines 63) not a packaged chip module are connected or bonded to a substrate. On the comments in page 3 of the Office Action dated 5/23/02, the Examiner also admits that it has been obvious that the chip of Venkateshwaran et al. is a **bare chip**.

Akram et al. teach a semiconductor package comprising multiple stacked substrates having flip chips attached to the substrates with chip on board assembly techniques to achieve dense packaging. As can be seen in the disclosure of Akram et al., a plurality of **first semiconductor dice 128 (col. 6, line 13), a plurality of second semiconductor dice 150 (col. 6, line 38), ..., or a plurality of fourth semiconductor dice 474 (col. 8, line 23), ...** rather than **a packaged chip module as claimed in claims 41 and 49** is used in the stacked substrate chip assembly.

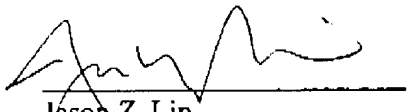
Chiang et al. disclose a semiconductor package comprising a chip which is tested by function test and burn-in test (col. 5, lines 64-67). The semiconductor package structure of Chiang et al., however, also comprises **a bare semiconductor chip. The concept of forming a multi-chip package by packaging already finished chip packages has not been discussed or anticipated.**

None of the cited prior arts has taught or suggested **packaging an already packaged chip module which has an embedded bare die, burn-in tested and function tested to form a multi-chip package structure**. Therefore, a person having ordinary

skill in the art can not reach the subject matter of the invention even if all the cited prior arts are combined.

From the foregoing discussion, it is clear that the instant invention differs from the cited prior arts. The physical difference results in different effects and is not obvious. The amended base claims 41 and 49 have clearly defined the unique feature of this invention and overcome all the rejections 35 U.S.C. §103(a) and should be patentable. By virtue of dependency, claims 40-45, 47-48 and 50-54, 56-57 should also be patentable. **A Credit Card Payment Form PTO-2038 in the amount of $740.00 to cover the Large Entity RCE fee.** Prompt and favorable reconsideration of the application is respectfully solicited.

Respectfully submitted,



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Version with Markings to Show Changes Made

CLAIMS:

41. (Amended) A multi-chip module package structure comprising:

a substrate;

at least two chip packages, each of said chip packages being a packaged chip module having a bare chip packaged and embedded therein, burn-in tested and function tested;

a plurality of electrical connect points electrically connecting said chip packages with said substrate;

a plurality of electrical connect pins; and

a package material enclosing said substrate, said connect points and said chip packages.

49. (Amended) A multi-chip module package structure comprising:

a substrate;

at least a bare chip;

at least one chip package, said chip package being a packaged chip module having a bare chip packaged and embedded therein, burn-in tested and function tested;

a plurality of electrical connect points electrically connecting said bare chip and said at least one chip package with said substrate;

a plurality of electrical connect pins; and

a package material enclosing said substrate, said connect points, said bare chip and said at least one chip package.